UNIVERSIDADE ESTADUAL DO OESTE DO PARANÁ - UNIOESTE

CENTRO DE ENGENHARIAS E CIÊNCIAS EXATAS - CECE

CIÊNCIA DA COMPUTAÇÃO

DISCIPLINA: SISTEMAS DIGITAIS

DOCENTES: JORGE HABIB E ANTONIO HACHISUCA

ISABELA PIMENTEL LOEBEL

LISTA DE EXERCÍCIOS 3 -

DESCREVENDO CIRCUITOS LÓGICOS

FOZ DO IGUAÇU,

2020.

# **Parte I - Livro Ronald J. Tocci**

B 3.26 Simplifique cada uma das seguintes expressões usando os teoremas de DeMorgan.

(a)

(b)

(c)

(d)

(e)

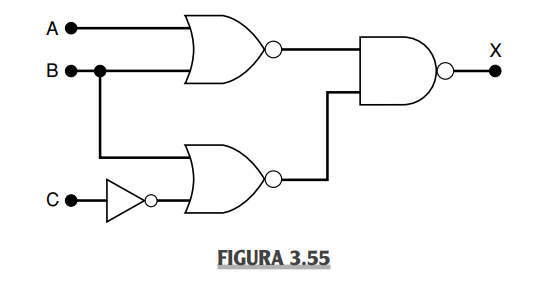
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(g)

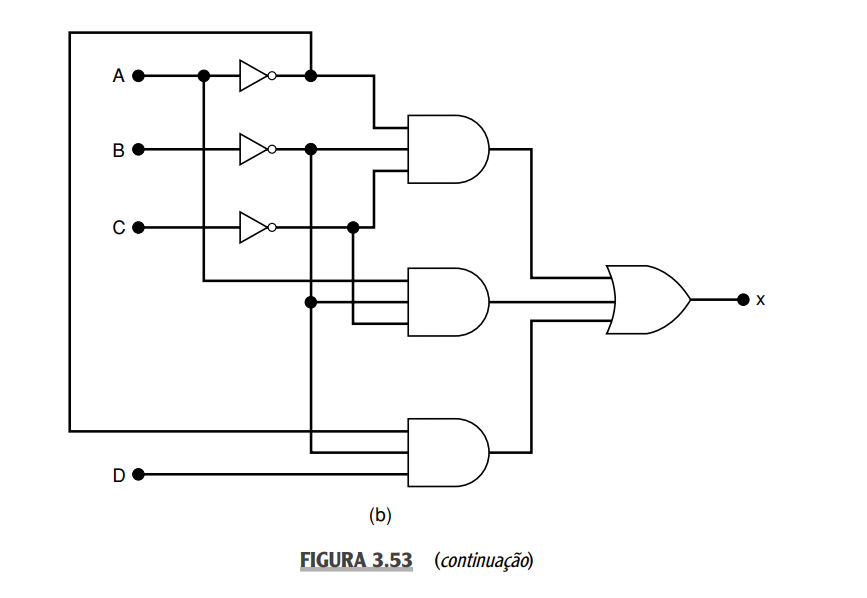
(h)

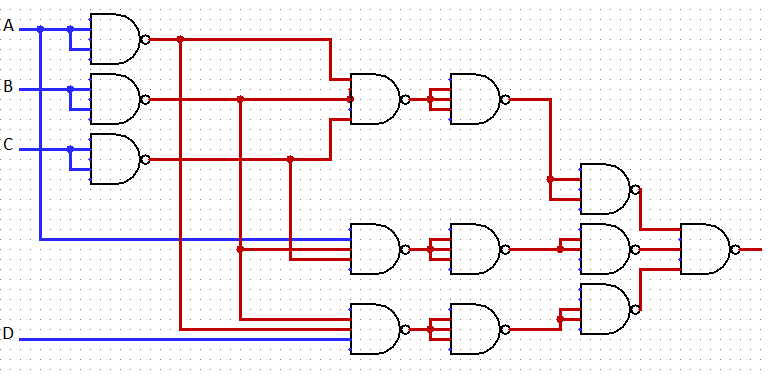
(i)

B 3.27\* Use os teoremas de DeMorgan para simplificar a expressão de saída do circuito da Figura 3.55.

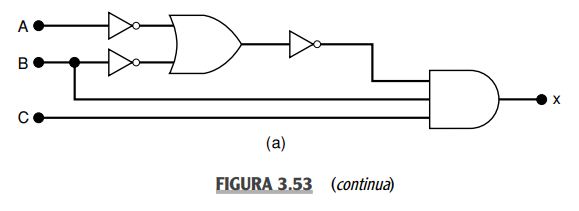


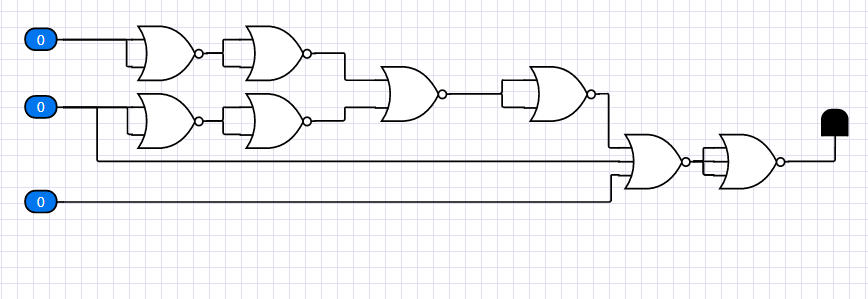
C 3.28 Converta o circuito da Figura 3.53(b) para um circuito que use apenas portas NAND. Em seguida, escreva a expressão de saída para o novo circuito, simplifique-a usando os teoremas de DeMorgan e compare-a com a expressão do circuito original.





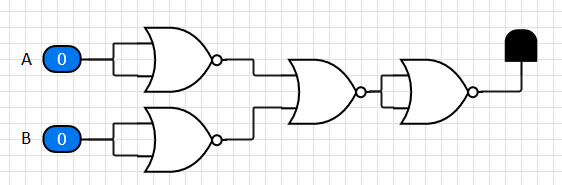
C 3.29 Converta o circuito da Figura 3.53(a) para um que use apenas portas NOR. Em seguida, escreva a expressão de saída para o novo circuito, simplifique-a usando os teoremas de DeMorgan e compare-a com a expressão do circuito original.





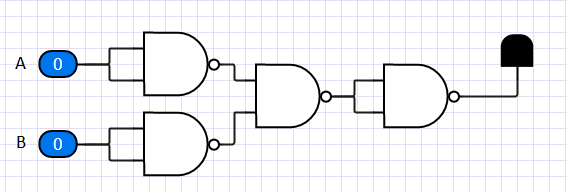
[Teste o circuito aqui.](http://circuits-cloud.com/circuit/details/LmfxFVnOCtAMnYv@SGec7aH@wprV17JMsYj8UFWw9wivuMnotB)

B 3.30 Mostre como uma porta NAND de duas entradas pode ser construída a partir de portas NOR de duas entradas.



[Teste o circuito aqui.](http://circuits-cloud.com/circuit/details/NbO08ImUDsS=Fj=VhQt5jTEzt$E3tZKgayhjhCeT47zKrdFG38)

B 3.31 Mostre como uma porta NOR de duas entradas pode ser construída a partir de portas NAND de duas entradas.



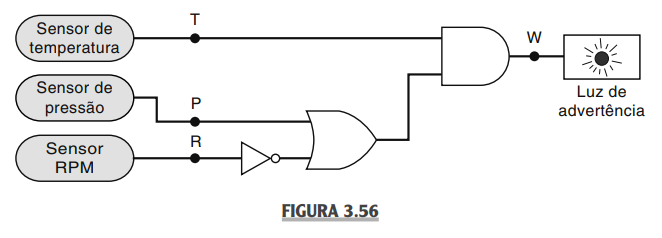
[Teste o circuito aqui.](http://circuits-cloud.com/circuit/details/X06KBVMwTDFgqy$DCSQ3usFu0KVHY7KW7QGIMseF4TVt$n62gV)

C 3.32 Um avião a jato emprega um sistema de monitoração dos valores de rpm, pressão e temperatura dos seus motores usando sensores que operam, conforme descrito a seguir:

saída do sensor RPM = 0 apenas quando a velocidade for < 4.800 rpm

saída do sensor P = 0 apenas quando a pressão for < 1,33 N/m2

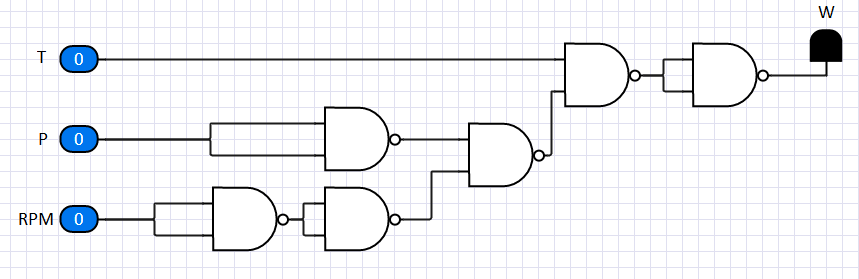
saída do sensor T = 0 apenas quando a temperatura for < 93,3°C

A Figura 3.56 mostra o circuito lógico que controla uma lâmpada de advertência dentro da cabine para certas combinações de condições da máquina. Admita que um nível ALTO na saída W ative a luz de advertência.

(a)\* Determine quais condições do motor indicam sinal de advertência ao piloto.

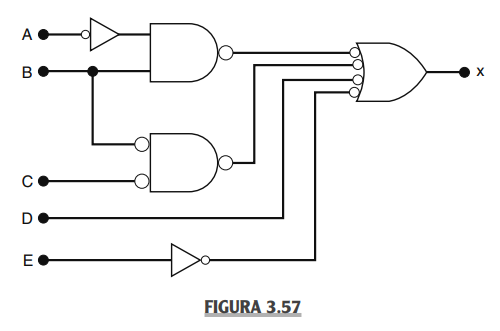
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| 1 | 1 | 1 | 0 | 1 | 1 |

(b) Troque esse circuito por outro que contenha apenas portas NAND.



[Teste o circuito aqui.](http://circuits-cloud.com/circuit/details/6uoqjwaOwTxKCvWzffxC@$ZMBNmIliXrLlQ4RZSnTq7vT349jB)

B 3.38\* Determine as condições de entrada necessárias para levar a saída para o estado ativo na Figura 3.57. & B 3.40 Use o resultado do Problema 3.38 para obter a tabela-verdade completa para o circuito da Figura 3.57.

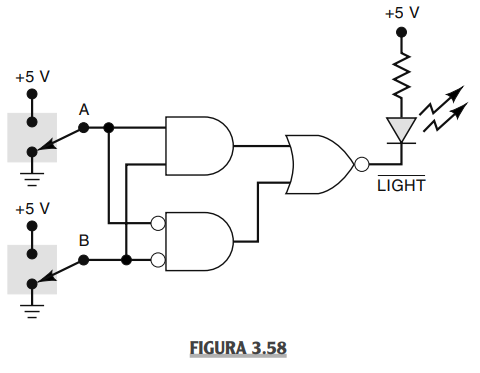


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| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |

B 3.39\* (a) Qual é o estado acionado (ativo) para a saída da Figura 3.57?

R: Se a saída x é 1.

N 3.41\* A Figura 3.58 mostra uma aplicação de portas lógicas que simula um circuito two-way como o usado em nossas casas para ligar ou desligar uma lâmpada a partir de interruptores diferentes. Nesse caso, é usado um LED que estará LIGADO (conduzindo) quando a saída da porta NOR for nível BAIXO. Observe que essa saída foi nomeada LIGHT para indicar que é ativa-em-baixo. Determine as condições de entrada necessárias para ligar o LED. Em seguida, verifique se o circuito funciona como um interruptor two-way (interruptores A e B). No Capítulo 4, você aprenderá a projetar circuitos como esse para produzir uma relação entre entradas e saídas.



R: Este circuito é utilizado para settar o LED/lâmpada para o estado contrário do atual settado. Como por exemplos, em quartos onde há dois ou mais interruptores em lados opostos do cômodo.

# **Parte II - Livro Thomas L. Floyd**

1. The output expression for an AND-OR circuit having one AND gate with inputs A, B and C and one AND gate with inputs D, E and F is:

(a) ABCDEF

(b) A + B + C + D + E + F

(c) ABC + DEF

(d) (A + B + C)(D + E + F)

2. A logic circuit with an output consists of:

(a) two AND gates and one OR gate

(b) two AND gates, one OR gate and an inverter

(c) two AND gates, two OR gates and two inverters

(d) two AND gates, one OR gate and three inverters

3. To implement the expression , it takes:

(a) five AND gates, one OR gate, and eight inverters

(b) four AND gates, two OR gates, and six inverters

(c) five AND gates, three OR gates, and seven inverters

(d) five AND gates, one OR gate, and seven inverters

4. The expression:

(a) cannot be simplified

(b) can be simplified to ABC + AB

(c) can be simplified to ABCD + ABC

(d) None of these answers is correct.

5. The output expression for an AND-OR-Invert circuit having one AND gate with inputs A, B, C and another AND gate with inputs D, E, F is:

(a) ABC + DEF

(b) (A + B + C)(D + E + F)

(c) (A + B + C)(D + E + F)

(d) A + B + C + D + E + F

6. An exclusive-NOR function is expressed as:

(a)

(b) AB + AB

(c) (A + B)(A + B)

(d) (A + B)(A + B)

7. The AND operation can be produced with:

(a) two NAND gates

(b) three NAND gates

(c) one NOR gate

(d) three NOR gates

8. The OR operation can be produced with:

(a) two NOR gates

(b) three NAND gates

(c) four NAND gates

(d) both answers (a) and (b)

9. When using dual symbols in a logic diagram,

(a) bubble outputs are connected to bubble inputs

(b) the NAND symbols produce the AND operations

(c) the negative-OR symbols produce the OR operations

(d) All of these answers are true.

(e) None of these answers is true.

10. All Boolean expressions can be implemented with:

(a) NAND gates only

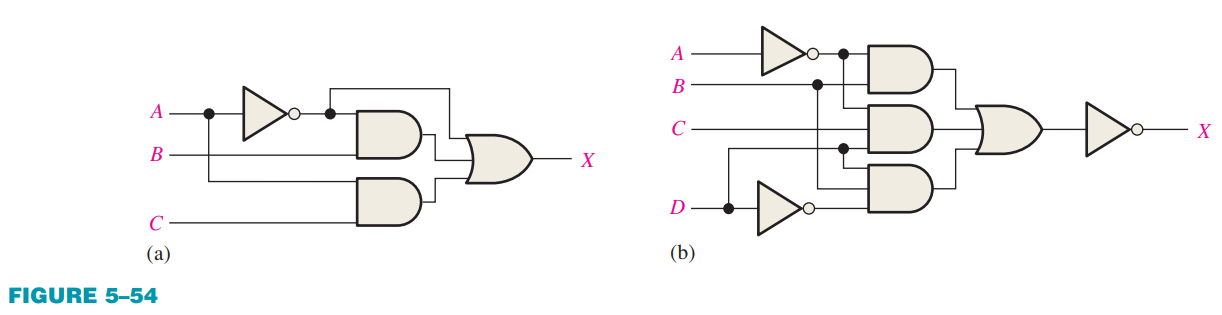
(b) NOR gates only

(c) combinations of NAND and NOR gates

(d) combinations of AND gates, OR gates, and inverters

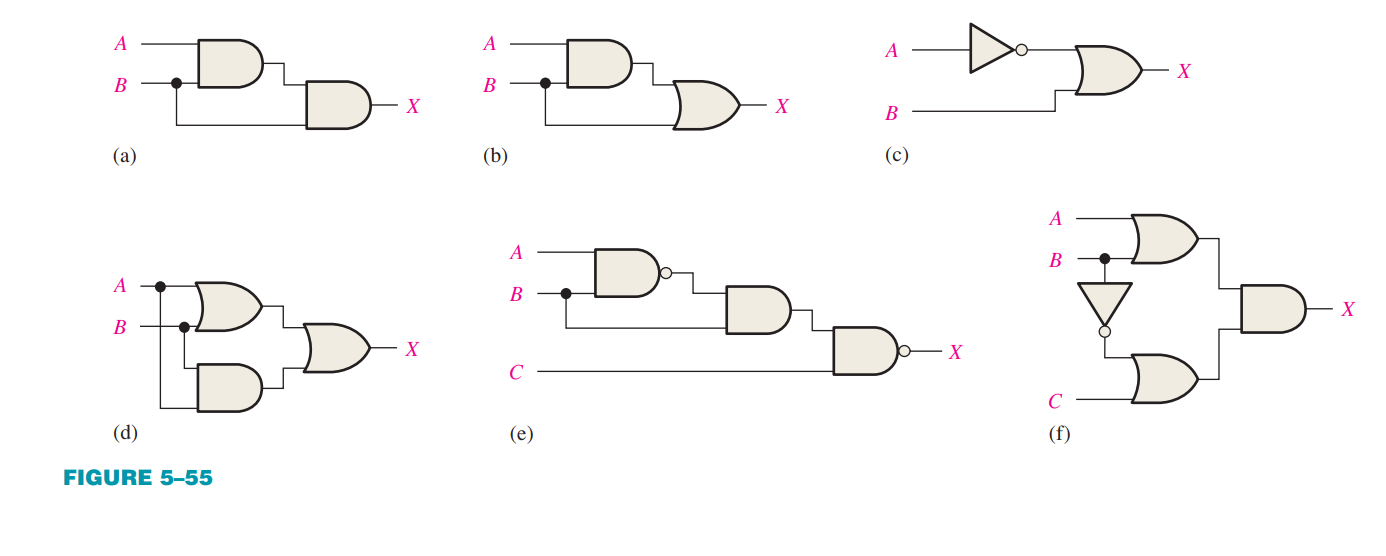
(e) any of these

2. Write the output expression for each circuit in Figure 5–54.

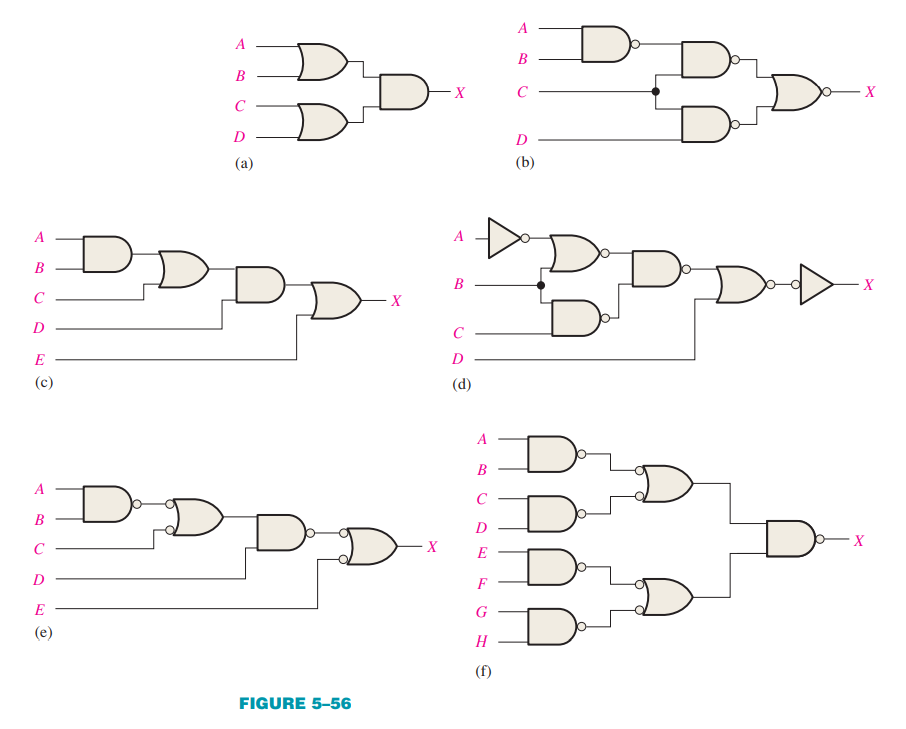


1. R: b) R:

3. Write the output expression for each circuit as it appears in Figure 5–55.



4. Write the output expression for each circuit as it appears in Figure 5–56 and then change each circuit to an equivalent AND-OR configuration.



5. Develop the truth table for each circuit in Figure 5–55.

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6. Develop the truth table for each circuit in Figure 5–56.

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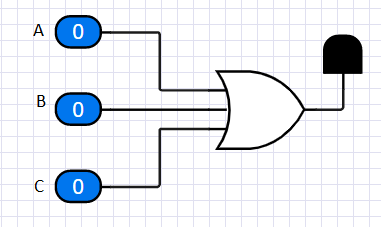
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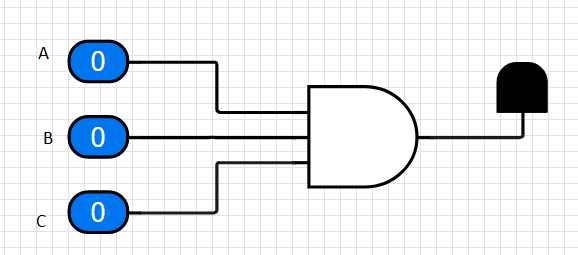
10. Use AND gates, OR gates, or combinations of both to implement the following logic expressions as stated:

(a) X = A + B + C



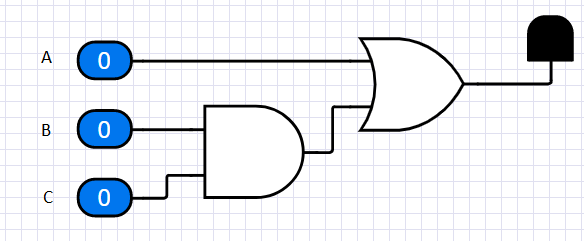
[Teste o circuito aqui.](http://circuits-cloud.com/circuit/details/PN6@7Ns$VIGM6MlDoLAz84wiv7VlnpzbcF3jsvJpeqalcvWAgw)

(b) X = ABC



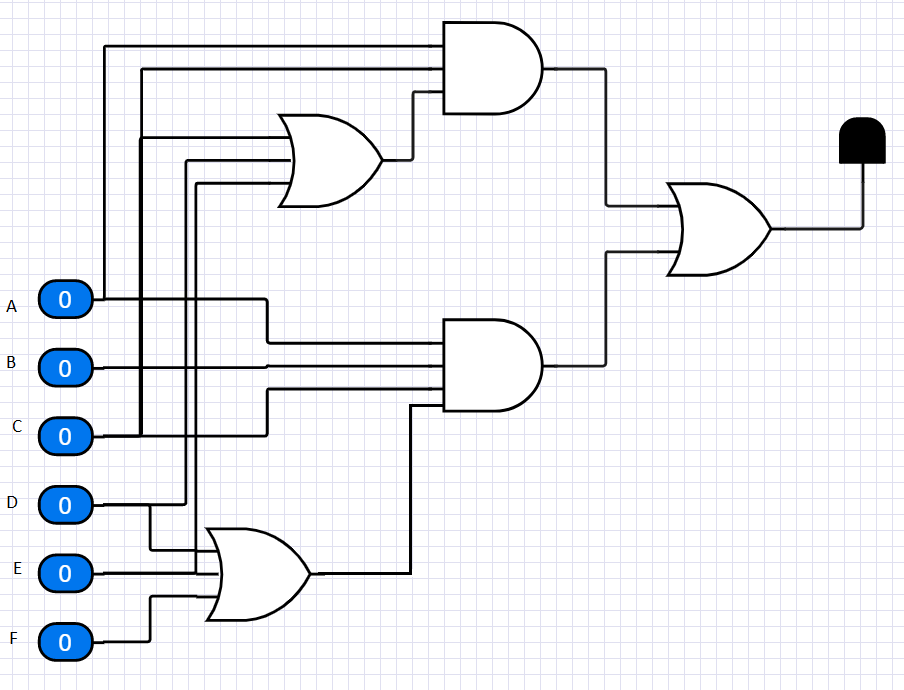
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(c) X = A + BC



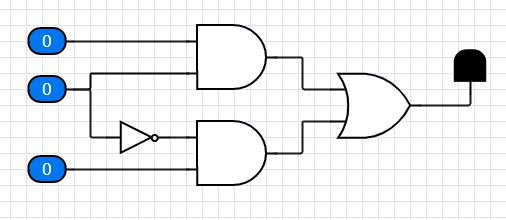
[Teste o circuito aqui.](http://circuits-cloud.com/circuit/details/e5JzXgYIeBmfV6vvalEI6wy5FbR8OOE2SoBRDAzQaT450ABaTe)

(h) X = ABC(D + E + F) + AC(C + D + E)



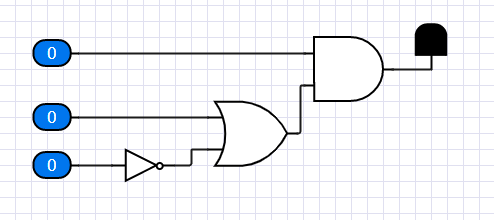
11. Use AND gates, OR gates, and inverters as needed to implement the following logic expressions as stated:

(a)



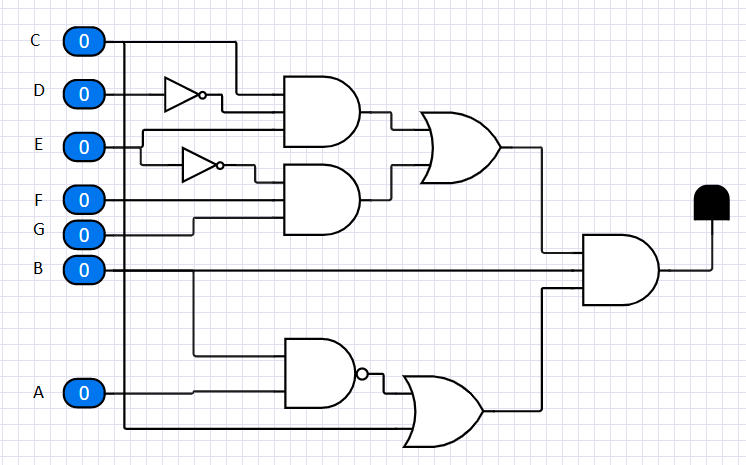
[Teste o circuito aqui.](http://circuits-cloud.com/circuit/details/OaLLTJ7XiF3$BOgG1epv0xVaDe5TIOKxYwi@gqPx4SYFGenIsK)

(b)



[Teste o circuito aqui.](http://circuits-cloud.com/circuit/details/5fv3VlMpKQth1esDrf@NA7khPBy30ER6@m9NFUcrKFGMS8pkoh)

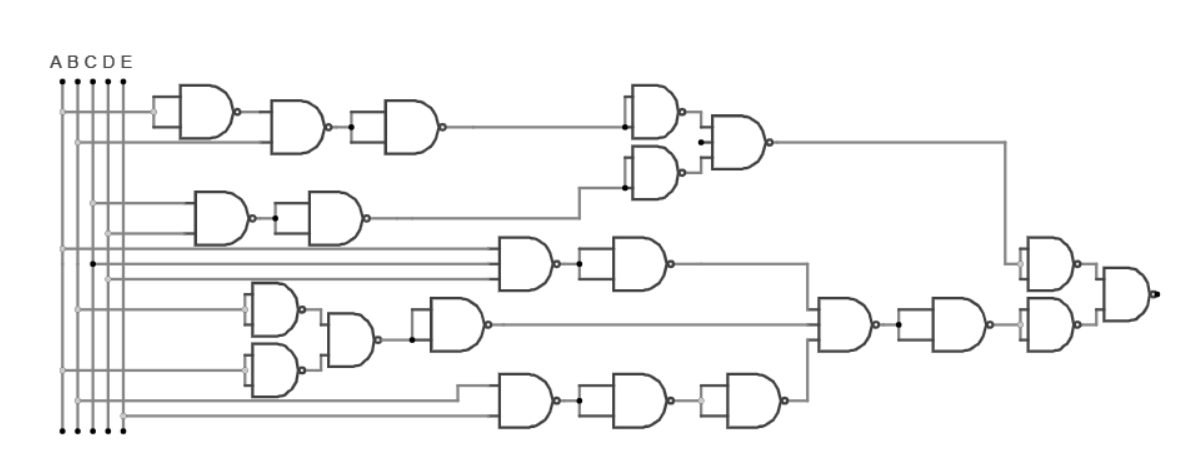
(f)



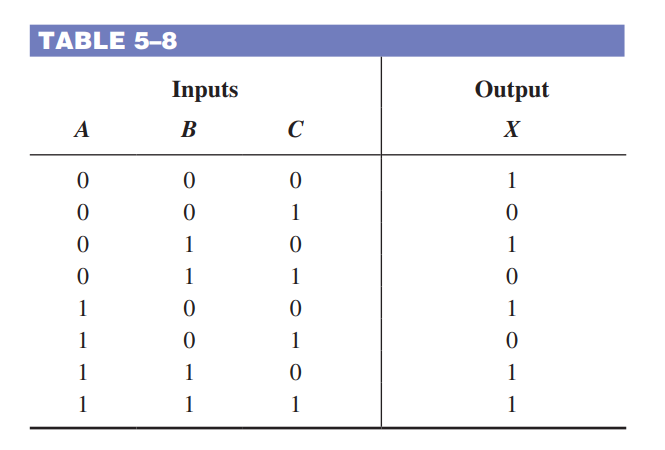
[Teste o circuito aqui.](http://circuits-cloud.com/circuit/details/j1xSm55EJ@CvFYL3nBsO85K4xV7qWZ6g1E8nJeZt5CXLAIOVjg)

12. Use NAND gates, NOR gates, or combinations of both to implement the following logic expressions as stated:

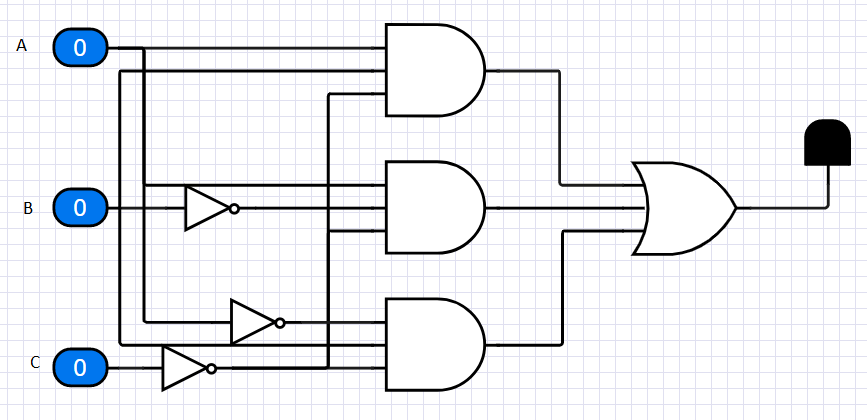
a)



13. Implement a logic circuit for the truth table in Table 5–8.

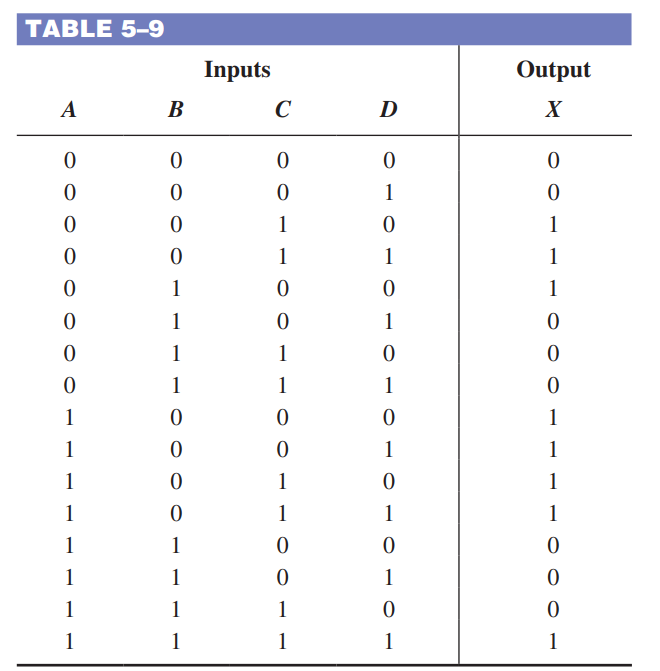


\*Agrupando os 0.

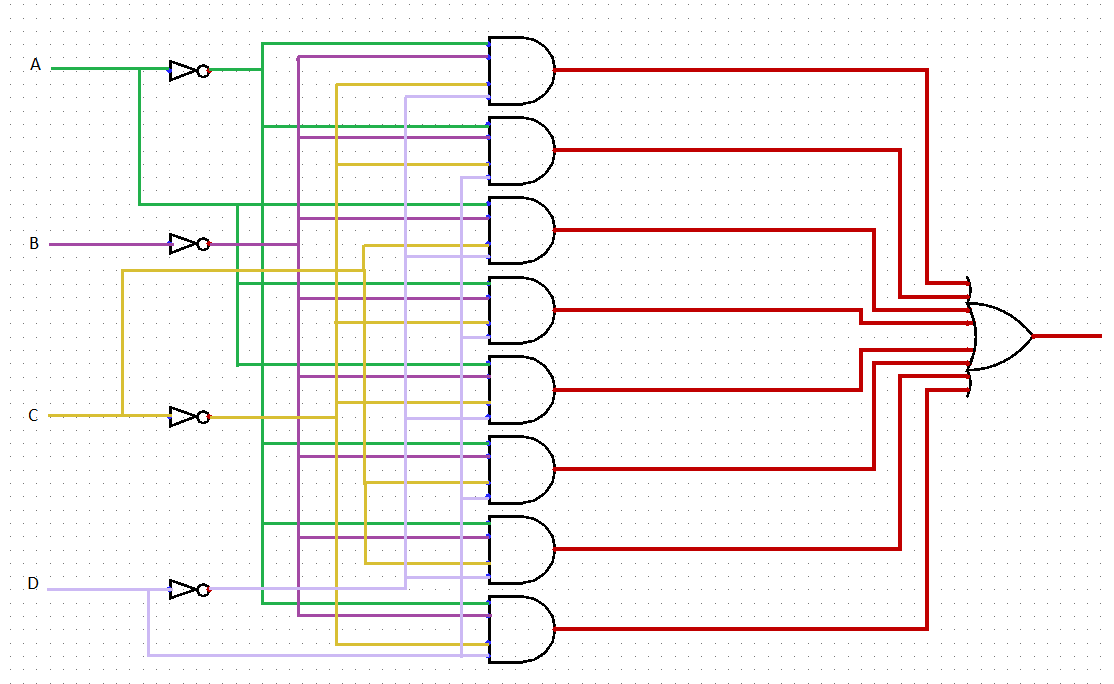


[Teste o circuito aqui.](http://circuits-cloud.com/circuit/details/WQs0vOPfamA9tUjVcJBVBkscgl5JHT7=KzFfouuxP4FjYXfaHP)

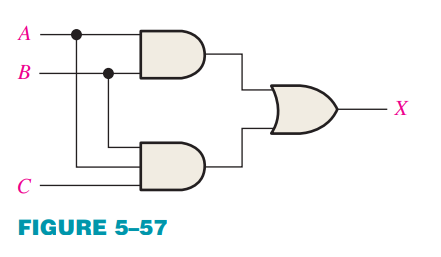
14. Implement a logic circuit for the truth table in Table 5–9.



\*Agrupando os 0.



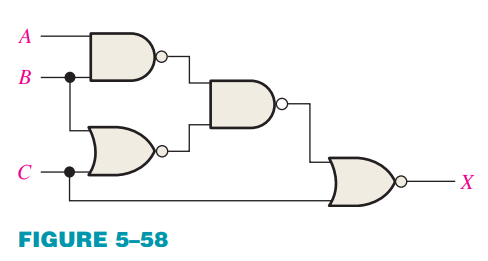
15. Simplify the circuit in Figure 5–57 as much as possible, and verify that the simplified circuit is equivalent to the original by showing that the truth tables are identical.



→

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

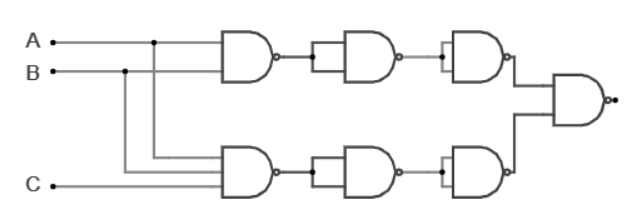
16. Repeat Problem 15 for the circuit in Figure 5–58.



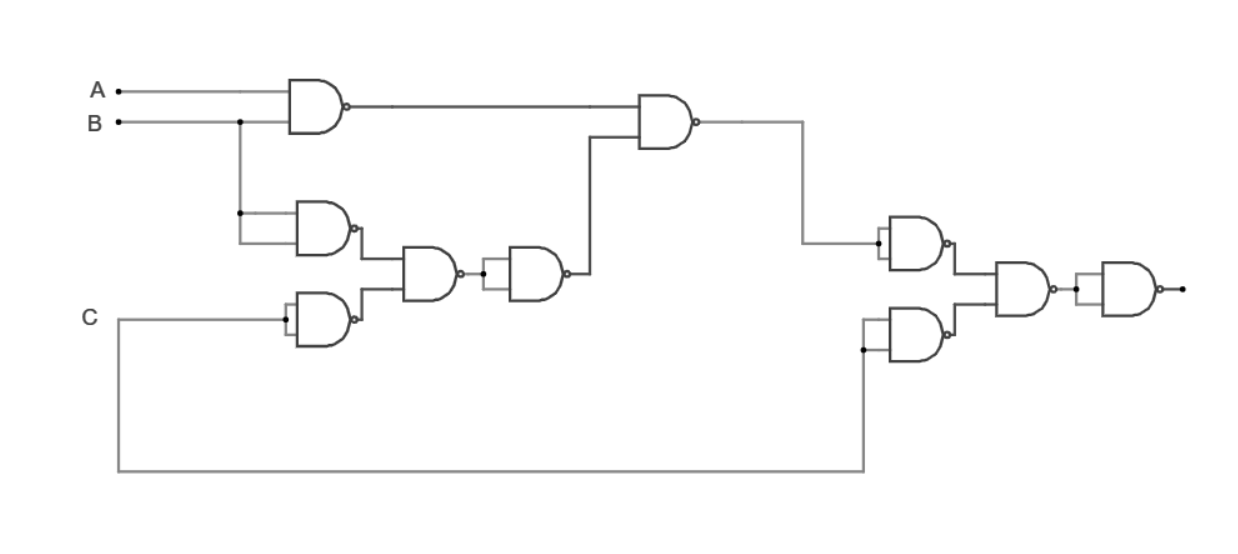
→

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 |

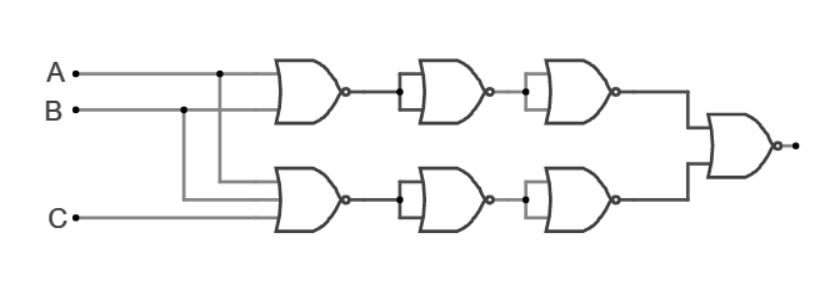
20. Implement the logic circuits in Figure 5–54 using only NAND gates.



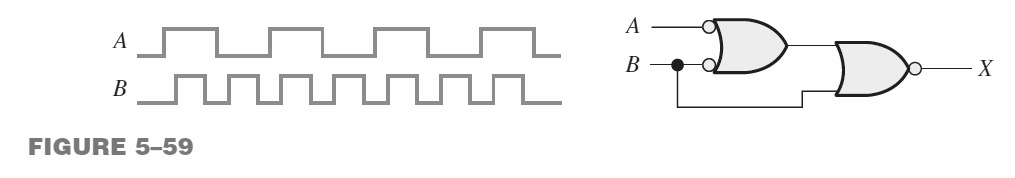
21. Implement the logic circuit in Figure 5–58 using only NAND gates.

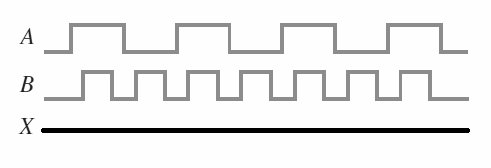


22. Repeat Problem 20 using only NOR gates.

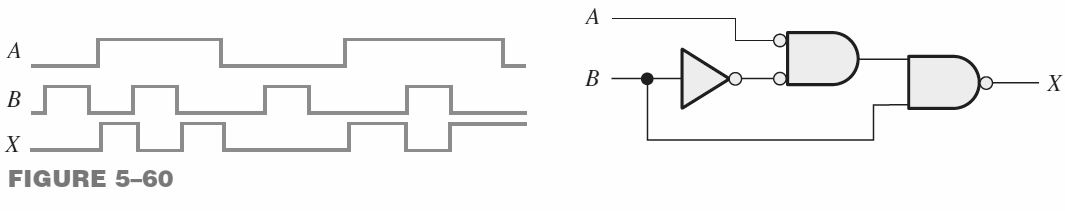


28. The output of the logic circuit and input waveforms in Figure 5–59 is passed through an inverter. Draw the output waveform.

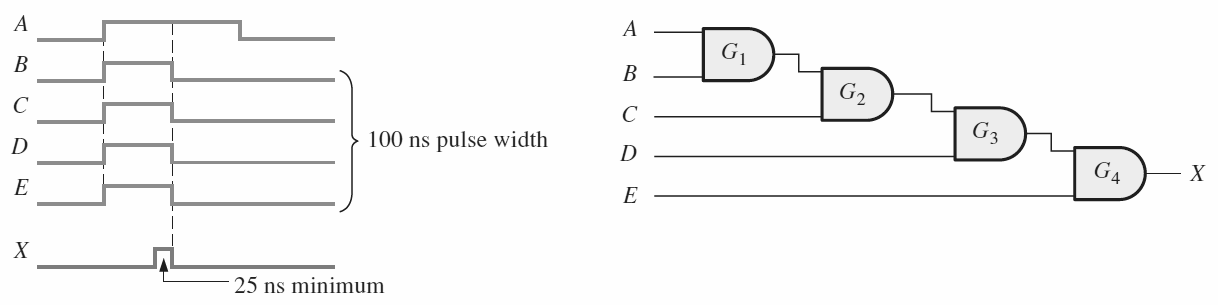




29. For the logic circuit in Figure 5–60, draw the output waveform in proper relationship to the inputs.



33. Assuming a propagation delay through each gate of 10 nanoseconds (ns), determine if the desired output waveform X in Figure 5–64 (a pulse with a minimum tW 5 25 ns positioned as shown) will be generated properly with the given inputs.



Não, pois é necessário que as entradas B, C, D e E ficarem mais tempo ligadas para que o delay de 10ns seja propagado entre as portas para que resulte em um espaço de tempo de 25 ns.